(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 655 834 A1**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **94118042.4**

(51) Int. Cl.6: **H03K 5/13**

(22) Date of filing: **15.11.94**

(30) Priority: **25.11.93 JP 317503/93**

(43) Date of publication of application:
31.05.95 Bulletin 95/22

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **NEC CORPORATION**
7-1, Shiba 5-chome
Minato-ku
Tokyo (JP)

(72) Inventor: **Furuchi, Masaki, c/o NEC Corporation**
7-1, Shiba 5-chome,
Minato-ku
Tokyo (JP)
Inventor: **Hirai, Masahiko, c/o NEC Corporation**
7-1, Shiba 5-chome,
Minato-ku
Tokyo (JP)

(74) Representative: **Glawe, Delfs, Moll & Partner**
Patentanwälte
Postfach 26 01 62
D-80058 München (DE)

(54) **Delay circuit using capacitor and transistor.**

(57) A delay circuit comprising at least one capacitor (209,210) with one electrode thereof is connected to a fixed potential (GND), a signal transmission line (212), and at least one switch means (205,208;211,206,207) between the other electrode of the capacitor and the signal transmission line (212). The switch means makes electrical connection or disconnection between the capacitor and the signal transmission line (212) in accordance with an actual supply voltage (Vdd) value.

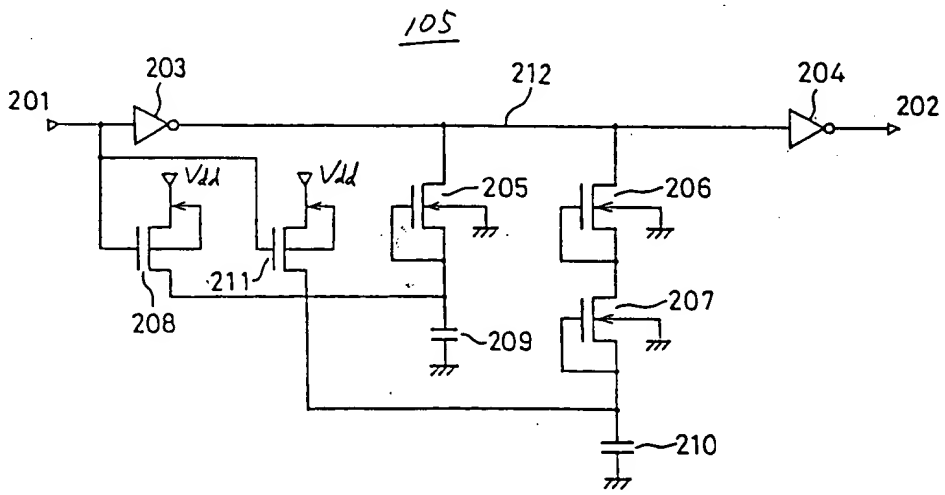

Fig. 2

EP 0 655 834 A1

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before describing the embodiments of the present invention, an application circuit of a delay circuit will be first described below with reference to Fig. 5. Shown in Fig. 5A is a two-phase clock generator having delay circuits according to the present invention. This generator includes a cross-coupled pair of circuits each including a two-input AND gate 106 (107) into one input of which a signal 101 (102) is supplied, a delay circuit 105 of which the output is connected to the other input of the AND gate 106 (107), and an inverter 108 (109) of which the output is connected to the delay circuit 105 and the input is connected to the output of the AND gate 107 (106). The output of the gates 106 and 107 are lead out as output terminals 103 and 104, respectively, which in turn generate two-phase clock signals. These clock signals are widely used as internal clocks of microcomputers.

Referring to the timing chart of Fig. 5B, the operation of the two-phase clock generator will be set forth. As understood from the chart, the two-phase clock generator generates, from a pair of input signals 101 and 102 having the inverted logic relationship to each other, two-phase clock signals 103 and 104 not overlapping during active high level period. That is, there are inactive low level periods as indicated by the reference numeral 110 between the two-phase clock output signals 103 and 104. These periods 110 are derived by masking the clock signals 101 or 102 by the output of each delay circuit 105 as determined by its delay time.

To implement the high-speed operation of the microcomputer, it is preferred to reduce the inactive low level period as short as possible without bringing a malfunction of the microcomputer.

Referring now to Fig. 2, the delay circuit 105 includes an input terminal 201 receiving the output of the inverter 108 (109) is connected to the input of an inverter 203. The output of the inverter 203 is connected to a signal transmission line 212 to another inverter 204 from which an output signal 202 is in turn derived. The line 212 is further connected an NMOS transistor 205 having the gate connected to the drain and further to a capacitor 209 which is grounded. The line 212 is also connected through two series-connected NMOS transistors 206 and 207 each with the gate connected to the drain to a capacitor 210 which is grounded. The input terminal 201 is further connected to the gate of a PMOS transistor 208 whose drain is connected to the node between the drain of the NMOS transistor 205 and the capacitor 209, and further to the gate of a PMOS transistor 211 whose drain connected to the node between the drain of the NMOS transistor 207 and the capacitor 210. The sources of these transistors 208 and 211 are connected to the power supply terminals Vdd. Each of the inverters 203 and 204 is a complementary MOS inverter consisting of a pair of PMOS and NMOS transistors similarly to the inverter gate 403 shown in Fig. 1.

The operation of the delay circuit of this embodiment will be described below. Firstly the operation will be described assumming that supply voltage Vdd is enough higher than twice the threshold voltage Vt of each of the NMOS transistors 205, 206 and 207.

When the input signal 201 is at low level, the output of the inverter 203 goes to the high level, thereby turning NMOS transistors 205, 206 and 207 off. Hereinafter, the high level is referred to as Vdd level, and the low level as GND level to distinguish that the high level is a potential varying with changing supply voltage Vdd.

On the other hand, the PMOS transistors 208 and 211 are turned on so that the capacitors 209 and 210 are charged to the Vdd level. The output 202 is at the GND level.

When the input signal 201 changes to Vdd level, both the PMOS transistors 208 and 211 are turned off, and the output of the inverter 203 changes from Vdd level to GND level, thus line 212 going to the GND level. Then all the gate-source voltages of the NMOS transistors 205, 206 and 207 exceeds the threshold voltage Vt, and consequently they are turned on.

Under the circumstances where the output of the inverter 203 is at GND level and hence the NMOS transistors 205, 206 and 207 are in the on-state, the charges accumulated on capacitors 209 and 210 are released through these NMOS transistors and the NMOS transistor (not shown) of the inverter 203, and consequently the line 212 will drop gradually to GND level.

When the line 212 reaches the GND level, output 202 is inverted to Vdd level but with delay of the time taken for the capacitors 209 and 210 to be discharged.

Next, the operation will be described assuming that supply voltage Vdd is somewhat higher than the threshold voltage Vt. When the input signal 201 is at GND level, the output of the inverter 203 goes to the Vdd level. Accordingly all the NMOS transistors 205, 206, 207 are turned off, and both PMOS transistors 208, 211 are turned on. Consequently the capacitors 209, 210 are charged. In this case the output 202 goes to the GND level.

Now, once the input signal 201 changes from the GND level to the Vdd level, both PMOS transistors 208, 211 are turned off, and the output of the inverter 203 goes to the GND level.

actual supply voltage so that the capacitance which are essential for determining the time constant can be finely adjusted. Tfius the variation in delay time associated with change of the supply voltage is remarkably reduced.

Additionally according to the present invention, one MOS transistor is provided between the capacitor and the signal transmission line so as to be turned off when the supply voltage is lower than the threshold voltage of the MOS transistor. This simplified construction can reduce the variation in the delay time depending on the supply voltage variation in a delay circuit needing no fine adjustment of the capacitance.

Claims

1. A delay circuit comprising a capacitor having a first electrode and a second electrode connected to a reference potential, a signal transmission line, and at least one switch element connected between the first electrode of said capacitor and said signal transmission line, said switch element being controlled to be conductive or nonconductive in accordance with a voltage representative of a level of a power supply voltage.

2. The circuit as claimed in claim 1, wherein said voltage is a voltage difference between said signal transmission line and said capacitor.

3. The circuit as claimed in claim 2, wherein said switch element comprises a transistor having a gate connected to the first electrode of said capacitor, said delay circuit further comprises means for charging, said capacitor while said transistor is being nonconductive.

4. The circuit as claimed in claim 1, said switching element comprises a transistor having a gate supplied with said power supply voltage.

5. A delay circuit comprising a capacitor having a first electrode and a second electrode connected to a reference potential, a signal transmission line, a drive circuit driving said signal in response to a signal applied thereto, a transistor having a gate supplied with a power supply voltage and a source-drain path connected between the first electrode of said capacitor and said signal transmission line.

6. The circuit as claimed in claim 5, wherein said transistor is of an N-channel type and has the gate supplied with said power supply voltage higher than said reference potential.

7. The circuit as claimed in claim 5, wherein said transistor is of a P-channel type and has the gate supplied with said reference potential as said power supply voltage.

8. A delay circuit comprising first and second capacitors each having a first electrode and a second electrode connected to a fixed potential, a signal line, a first switching circuit having at least one diode-connected transistor and coupled between said signal line and the second electrode of said capacitor, and a second switching circuit having at least two diode-connected transistors and coupled between said signal line and the second electrode of said second capacitor.

9. The circuit as claimed in claim 8, further comprising a drive circuit responding to a signal and driving said signal line, and a charging circuit responding to said signal and charging each of said first and second capacitors.

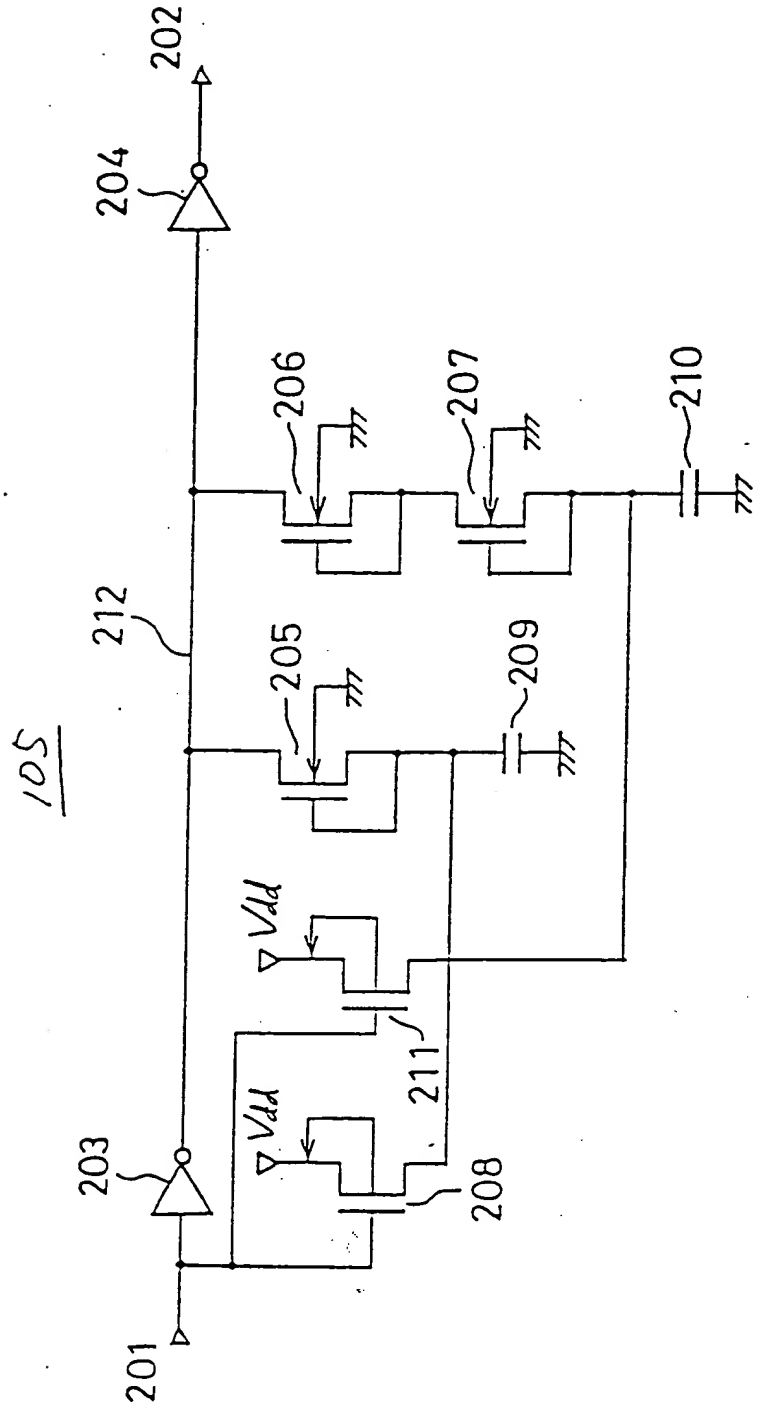

Fig. 2

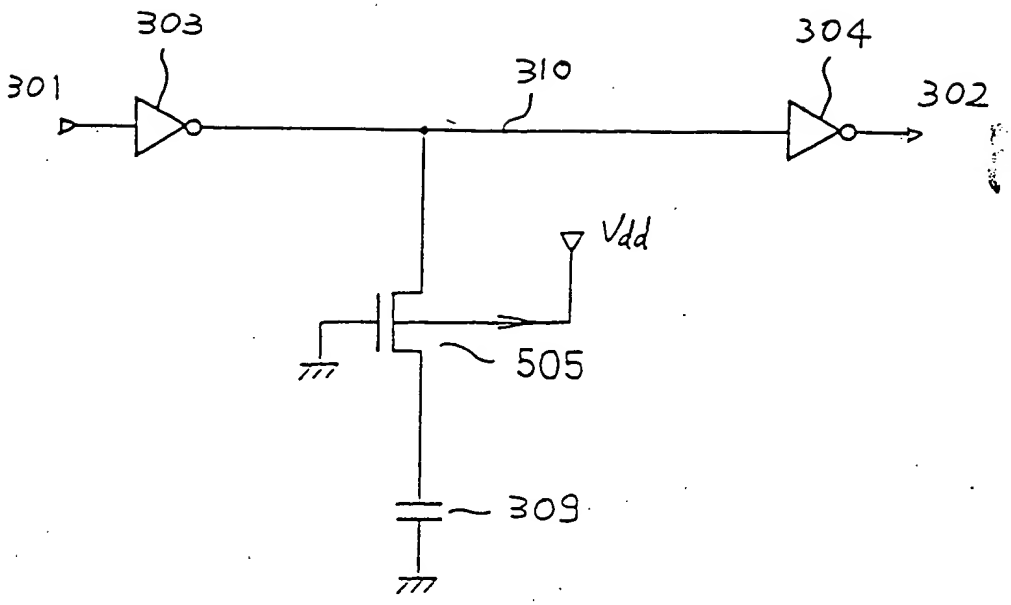

Fig. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 11 8042

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US-A-5 012 142 (SONNTAG JEFFREY L) 30 April 1991	1-3	H03K5/13
A	* column 3, line 34 - column 4, line 56; figures 2,3 *	4-9	
X	IEEE JOURNAL OF SOLID-STATE CIRCUITS, DEC. 1992, USA, vol. 27, no.12, ISSN 0018-9200, pages 1934-1940, BAZES M ET AL 'A novel CMOS digital clock and data decoder'	1-3	
A	* figure 5 *	4-9	
P,X	US-A-5 287 025 (NISHIMICHI YOSHITO) 15 February 1994 * column 7, line 31 - line 39; figure 1 *	1-3	
X	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 35, no.4a, September 1992 NEW YORK US, pages 365-366, XP 000314796 'variable delay circuit' * the whole document *	1-3	
P,A	DE-A-43 30 600 (HITACHI LTD) 17 March 1994 * figures 1-4 *	1-9	
A	US-A-5 180 938 (SIN YUN-SEUNG) 19 January 1993		

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	7 March 1995	Segaert, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)